AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (currently amended): A European digital audio broadcast receiver having diverse fast Fourier transform (FFT) modes based on sizes of transmitted data, comprising:

an address generator for generating a number of write addresses, wherein the number of write addresses is determined prior to the European digital audio broadcast receiver receiving the transmitted data;

a fast Fourier transform (FFT) processor for repeating data of FFT modes to generate a predetermined number of data and implementing a fast Fourier transform (FFT) by using the predetermined number of data; and

a controller for controlling the address generator to generate a number of read addresses according to operations of the FFT processor,

wherein the number of write addresses generated by the address generator is independent of the sizes of the transmitted data.

2. (original): The receiver as claimed in claim 1, wherein the predetermined number of data is 4096, and the FFT processor uses the 4096 data to implement the fast Fourier transform.

3. (previously presented): The receiver as claimed in claim 1, wherein the FFT processor includes:

a memory controller for repeating the data of FFT modes to generate 4096 data;

a memory having a size capable of storing 2048 data; and

an algorithm unit for using the 4096 data and implementing Radix-4 based operations on the 4096 data to generate Radix-4 implemented data that is stored in the memory, and,

in the case that the read addresses are generated, the memory controller digit-reverses the addresses of the memory to correspond to the generated read addresses.

4. (previously presented): The receiver as claimed in claim 3, wherein the memory controller has a virtual memory storing data other than the 2048 data stored in the memory in order for the algorithm unit to implement the Radix-4 based operations.

5. (original): The receiver as claimed in claim 4, wherein the algorithm unit implements the Radix-4 based operations, and, accordingly, "0" data blocks are stored in the virtual memory in correspondence to the FFT modes.

6. (previously presented): The receiver as claimed in claim 3, wherein the memory controller digit-reverses the Radix-4 implemented data stored in the memory corresponding to the FFT modes.

7. (original): The receiver as claimed in claim 3, wherein, in the case that a bit array of the read addresses from a highest bit to a lowest bit has $\{a_{11}, a_{10}, a_9, a_8, a_7, a_6, a_5, a_4, a_3, a_2, a_1, a_0\}$ in 2048 FFT mode, the memory controller digit-reverses the bit array of the memory addresses from the highest bit to the lowest bit into $\{a_1, a_3, a_2, a_5, a_4, a_7, a_6, a_9, a_8, a_{11}, a_{10}\}$.

8. (original): The receiver as claimed in claim 3, wherein, in the case that a bit array of the read addresses from a highest bit to a lowest bit has $\{a_{11}, a_{10}, a_9, a_8, a_7, a_6, a_5, a_4, a_3, a_2, a_1, a_0\}$ in 1024 FFT mode, the memory controller digit-reverses the bit array of the memory addresses from the highest bit to the lowest bit into $\{0, a_3, a_2, a_5, a_4, a_7, a_6, a_9, a_8, a_{11}, a_{10}\}$.

9. (original): The receiver as claimed in claim 3, wherein, in the case that a bit array of the read addresses from a highest bit to a lowest bit has $\{a_{11}, a_{10}, a_9, a_8, a_7, a_6, a_5, a_4, a_3, a_2, a_1, a_0\}$ in 256 FFT mode, the memory controller digit-reverses the bit array of the memory addresses from the highest bit to the lowest bit into $\{0, 0, 0, a_5, a_4, a_7, a_6, a_9, a_8, a_{11}, a_{10}\}$.

10. (original): The receiver as claimed in claim 3, wherein, in the case that a bit array of the read addresses from a highest bit to a lowest bit has $\{a_{11}, a_{10}, a_9, a_8, a_7, a_6, a_5, a_4, a_3, a_2, a_1, a_0\}$ in 512 FFT mode, the memory controller digit-reverses the bit array of the memory addresses from the highest bit to the lowest bit into $\{0, a_3, 0, a_5, a_4, a_7, a_6, a_9, a_8, a_{11}, a_{10}\}$.

11. (currently amended): An operation method for a European digital audio broadcast receiver having diverse FFT modes based on sizes of transmitted data, comprising:

generating a number of write addresses, wherein the number of write addresses is determined prior to the European digital audio broadcast receiver receiving the transmitted data;

repeating data of FFT modes to generate a predetermined number of data in correspondence to the generated write addresses,

implementing a fast Fourier transform (FFT) by using the predetermined number of data; and

generating read addresses if the implementing the FFT is completed,

wherein the generating the number of write addresses comprises generating the number of write addresses independent of the sizes of the transmitted data.

12. (previously presented): The operation method as claimed in claim 11, wherein the predetermined number of data is 4096, and the implementing the FFT uses the 4096 data to implement the fast Fourier transform.

13. (previously presented): The operation method as claimed in claim 11, wherein the implementing the FFT includes:

repeating the data of FFT modes to generate 4096 data;

using the generated 4096 data to implement Radix-4 based operations to generate Radix-4 implemented data, and storing the Radix-4 implemented data in a memory in correspondence to write addresses of the memory; and

in the case that the read addresses are generated, digit reversing the addresses of the memory to correspond to the generated read addresses.

14. (previously presented): The operation method as claimed in claim 13, further comprising:

storing the Radix-4 implemented data in the memory and a virtual memory,

wherein the memory is capable of storing 2048 data.

15. (previously presented): The operation method as claimed in claim 14, wherein the using the 4096 data implements the Radix-4 based operations, and, accordingly, "0" data blocks are stored in the virtual memory in correspondence to the FFT modes.

16. (previously presented): The operation method as claimed in claim 13, wherein the digit-reversing digit-reverses the addresses of the Radix-4 implemented data stored in the memory corresponding to the FFT modes.

17. (previously presented): The operation method as claimed in claim 13, wherein, in the case that a bit array of the read addresses from a highest bit to a lowest bit has $\{a_{11}, a_{10}, a_9, a_8, a_7, a_6, a_5, a_4, a_3, a_2, a_1, a_0\}$ in 2048 FFT mode, the digit-reversing digit-reverses the bit array of the memory addresses from the highest bit to the lowest bit into $\{a_1, a_3, a_2, a_5, a_4, a_7, a_6, a_9, a_8, a_{11}, a_{10}\}$.

18. (previously presented): The operation method as claimed in claim 13, wherein, in the case that a bit array of the read addresses from a highest bit to a lowest bit has $\{a_{11}, a_{10}, a_9, a_8, a_7, a_6, a_5, a_4, a_3, a_2, a_1, a_0\}$ in 1024 FFT mode, the digit-reversing digit-reverses the bit array of the memory addresses from the highest bit to the lowest bit into $\{0, a_3, a_2, a_5, a_4, a_7, a_6, a_9, a_8, a_{11}, a_{10}\}$.

19. (previously presented): The operation method as claimed in claim 13, wherein, in the case that a bit array of the read addresses from a highest bit to a lowest bit has $\{a_{11}, a_{10}, a_9, a_8, a_7,$

a_6, a_5, a_4, a_3, a_2, a_1, a_0} in 256 FFT mode, the digit-reversing digit-reverses the bit array of the memory addresses from the highest bit to the lowest bit into {0, 0, 0, a_5, a_4, a_7, a_6, a_9, a_8, a_{11}, a_{10}}.

20. (previously presented): The operation method as claimed in claim 13, wherein, in the case that a bit array of the read addresses from a highest bit to a lowest bit has {a_{11}, a_{10}, a_9, a_8, a_7, a_6, a_5, a_4, a_3, a_2, a_1, a_0} in 512 FFT mode, the digit-reversing digit-reverses the bit array of the memory addresses from the highest bit to the lowest bit into {0, a_3, 0, a_5, a_4, a_7, a_6, a_9, a_8, a_{11}, a_{10}}.

21. (currently amended): A receiver for processing data, the receiver comprising:

a receiving circuit that receives data;

a generating circuit that generates a number of write addresses if the receiving circuit receives the data, wherein the number of write addresses is determined prior to the receiving circuit receiving the data;

a processing circuit that processed the received data through fast Fourier transform modes to generate a first number of data corresponding to the generated predetermined number of write addresses, wherein the processing is repeated based on a size of the received data;

a fast Fourier transform circuit that implements a fast Fourier transform using the generated first number of data; and

a control circuit that controls the generating circuit to generate a number of read addresses according to operations of the fast Fourier transform circuit,

<u>wherein the number of write addresses generated by the generating circuit is independent of a number of the data received by the receiving circuit</u>.

22. (currently amended): A method for processing data in a receiver, the method comprising:

receiving data by a receiver;

generating a number of write addresses if the receiver receives the data, wherein the number of write addresses is determined prior to the receiving the data by the receiver;

processing the received data through fast Fourier transform modes to generate a first number of data corresponding to the generated predetermined number of write addresses, wherein the processing is repeated based on a size of the received data;

implementing a fast Fourier transform using the generated first number of data; and

generating read addresses if the implementing the fast Fourier transform is completed,

wherein the generating the number of write addresses comprises generating the number of write addresses independent of a number of the received data.